REMARKS

Claims 1 - 5, 7, 13, 14, 15 - 18 and 36 - 40 are pending in the Application, and claims 8 - 12 and 19 - 35 are cancelled.

ALLOWABLE SUBJECT MATTER

Applicants thank the Examiner for indicating allowable subject matter. Applicants have amended Claim 1 to include limitations from previous Claim 6 and respectfully assert Claim 1 is allowable. Applicants respectfully assert Claims 2 - 5 and 7 are allowable as depending from allowable independent Claim 1. Applicants have amended Claim 13 to include limitations from previous Claim 15 and respectfully assert Claim 13 is allowable. Applicants respectfully assert Claims 14 and 16 - 18 are allowable as depending from allowable independent Claim 13.

Applicants have added new claims 36 – 40. Applicants respectfully assert new independent Claim 36 is allowable at least for reasons similar to the indicated allowability of amended independent Claim 1, including the feature of a redistribution layer including a test signal redistribution layer trace for communicating internal signals to the conductive test signal bump, wherein the test signal redistribution layer trace is routed ***in a spiral pattern***.... Applicants

also respectfully assert Claims 27 – 40 are allowable at least as depending from allowable independent Claim 36.

102 REJECTIONS

The present Office Action indicates Claims 1, 3-5, 13, 14, and 18 are rejected under 35 U.S.C. 102 (b) as being anticipated by Motika et al. (US 5,807,763). Applicants respectfully assert that the present invention is neither shown nor suggested by the Motika et al. reference.

Applicants respectfully assert that the Motika et al. reference is not directed to the present invention as recited in Claim 1. Specifically the present invention, as set forth in independent Claim 1 recites in part:

> … a test probe point for accessing said test signals in said semiconductor die and for electrical coupling to said redistribution layer … .

To the extent the Motika et al. reference may show probes 146 that are ***external*** to the integrated circuit chip 102 ***die*** [Figure 1], Applicants respectfully assert the Motika et al. reference does not teach the a semiconductor ***die comprising*** a test ***probe point*** for accessing the test signals in the semiconductor die.

In addition, to the extent the Motika et al. reference may mention pads or bumps 140 may be provided over the passivation layer at the cavities, or the cavities may be made larger to expose pads of the wiring layers [Col. 6 lines19 - 22], Applicants respectfully assert the Motika et al. reference does not teach a test signal redistribution trace is disposed such that multiple test signals are ***accessible at varying degrees*** of electronic component granularity within the die and ***along*** the test signal redistribution layer trace. Applicants respectfully assert that no matter where a test point is moved along the redistribution trace it is limited to the same granularity as the pad 40 and thus the same ***unvarying*** granularity of electronic component access the corresponding bonding pad has to the internal circuitry.

Applicants respectfully assert Claims 2 – 5 and 7 are allowable as depending from allowable independent Claim 1.

In addition, with respect to Claim 5 to the extent the Motika et al. reference may mention a second wiring layer 134 [Col. 6 line 9 and Figure 1], Applicants respectfully assert the Motika et al. reference does not teach a test signal redistribution layer ***trace*** is ***dedicated*** for ***test*** signals.

Applicants respectfully assert that the Motika et al. reference is not directed to the present invention as recited in Claim 13. Specifically the present invention, as set forth in independent Claim 13 recites in part:

> ... a semiconductor die having test probe points accessible by said external access point, wherein said semiconductor die is electrically coupled to said package substrate ... .

To the extent the Motika et al. reference may mention pads or bumps 140 may be provided over the passivation layer at the cavities, or the cavities may be made larger to expose pads of the wiring layers [Col. 6 lines19 -22], Applicants respectfully assert the Motika et al. reference does not teach a test signal redistribution trace is disposed such that multiple test signals are ***accessible at varying degrees*** of electronic component granularity within the die and ***along*** the test signal redistribution layer trace. Applicants respectfully assert that no matter where a test point is moved along the redistribution trace it is limited to the same granularity as the pad 40 and thus the same ***unvarying*** granularity of electronic component access the corresponding bonding pad has to the internal circuitry.

Applicants respectfully assert Claims 14 and 16 - 18 are allowable as depending from allowable independent Claim 13.

CONCLUSION

In light of the above-listed amendments and remarks, Applicant respectfully request allowance of the remaining Claims. The examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Applicant respectfully petitions for a 1 Month extension of time under 37 C.F.R. 1.136 and is including the fee under 37 C.F.R. 1.17. If an additional extension of time is required, please consider this a petition therefore. Please charge and additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
Murabito, Hao & Barnes LLP

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